

1 **CLAIMS**

2 1. An apparatus comprising:

3 a delay-locked loop circuit to generate a first clock signal, the delay-locked
4 loop circuit including a first delay element coupled in a feedback path of the
5 delay-locked loop circuit to advance the first clock signal relative to a reference
6 clock signal by a first time period; and

7 a second delay element coupled to receive the first clock signal from the
8 delay-locked loop circuit and to output a second clock signal that is delayed
9 relative to the first clock signal by the first time period wherein the second delay
10 element is outside the feedback path.

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12 2. An apparatus as recited in claim 1 wherein the delay-locked loop
13 circuit further includes a phase detector to identify phase differences between the
14 first clock signal and the reference clock signal.

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16 3. An apparatus as recited in claim 2 wherein the phase detector is a
17 zero phase detector.

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19 4. An apparatus as recited in claim 2 wherein the phase detector is an
20 integration sampler to integrate the first clock signal with respect to the reference
21 clock signal.

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23 5. An apparatus as recited in claim 1 wherein the delay-locked loop
24 circuit further includes a 180 degree phase shifter to adjust the phase of the first
25 clock signal.

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2 6. An apparatus as recited in claim 1 wherein the first clock signal
3 indicates when to transmit data onto a data bus.

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5 7. An apparatus as recited in claim 1 wherein the second clock signal
6 indicates when to receive data from a data bus.

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8 8. An apparatus as recited in claim 1 wherein the second delay element is
9 separate from the delay-locked loop circuit.

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11 9. A method comprising:
12 generating a first clock signal using a delay-locked loop circuit;
13 advancing the first clock signal relative to a reference clock signal by a first
14 time period using a first delay element coupled in the feedback path of the delay-
15 locked loop circuit; and
16 generating a second clock signal that is delayed relative to the first clock
17 signal by the first time period using a second delay element coupled to receive the
18 first clock signal, wherein the second delay element is outside the feedback path of
19 the delay-locked loop circuit.

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21 10. A method as recited in claim 9 further including transmitting data
22 onto a data bus based on the state of the first clock signal.

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24 11. A method as recited in claim 9 further including receiving data from
25 a data bus based on the state of the first clock signal.

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2 **12.** A method as recited in claim 9 further including identifying the
3 phase differences between the first clock signal and the reference clock signal.
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5 **13.** A method as recited in claim 9 further including integrating the first
6 clock signal with respect to the reference clock signal.
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8 **14.** A memory system comprising:
9 a memory storage device;
10 a data bus coupled to the memory storage device; and
11 a memory controller coupled to the data bus, the memory controller
12 including:

13 a delay-locked loop circuit to generate a first clock signal, the delay-
14 locked loop circuit including a first delay element coupled in a feedback
15 path of the delay-locked loop circuit to advance the first clock signal
16 relative to a reference clock signal by a first time period; and

17 a second delay element coupled to receive the first clock signal from
18 the delay-locked loop circuit and to output a second clock signal that is
19 delayed relative to the first clock signal by the first time period, wherein the
20 second delay element is outside the feedback path.
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22 **15.** A memory system as recited in claim 14 wherein the delay-locked
23 loop circuit includes a phase detector to identify phase differences between the
24 first clock signal and the reference clock.
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1 **16.** A memory system as recited in claim 15 wherein the phase detector
2 is a zero phase detector.

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4 **17.** A memory system as recited in claim 15 wherein the phase detector
5 is an integration sampler to integrate the first clock signal against the reference
6 clock signal.

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8 **18.** A memory system as recited in claim 14 wherein the first clock
9 signal indicates when to transmit data onto the data bus.

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11 **19.** A memory system as recited in claim 14 wherein the second clock
12 signal indicates when to receive data from the data bus.

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14 **20.** A memory system as recited in claim 14 wherein the second delay
15 element is separate from the delay-locked loop circuit.